REMARKS

The claims are claims 1, 2, 4, 10, 11, 13 and 15 to 24.

The application has been further amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner.

Claims 1, 2, 10 and 11 have been amended. Claims 3, 5 to 9 and 14 are canceled. New claims 15 to 24 are added. Claims 1, 2, 10 and 11 are amended to distinguish over the rejection. New claims 15 and 20 recite that the instruction designates a general purpose register as the test register. New claims 16 and 21 recite that a general purpose register is the predicate register. Claims 17 and 22 recite that the predicate register is selected from a subset of the general purpose registers. Claims 18 and 23 recite that fetch packets of a predetermined plurality of instructions on predetermined address boundaries and that the branch address is the sum of the displacement and the predetermined address boundary of the last fetch packet. Claims 19 and 24 recite execute packets that can span fetch patch and that a conditional branch-decrement instruction in a latter fetch packet computes the branch address from the address boundary of the second fetch packet.

Claims 1, 2, 4, 10, 11 and 13 were rejected under 35 U.S.C. 102(b) as being anticipated by Black et al U.S. Patent No. 5,761,723.

Claims 1 and 10 recite subject matter not anticipated by Black et al. Claim 1 recites "decrement circuitry connected to receive the operand from the selected test register, and having an output connected to conditionally provide a decremented value of the operand to the test register dependent upon said indicated condition of the operand." Claim 10 recites "modifying the contents of the test register if the contents of the test register

meet the first condition." These recitations state that decrement or modification of the text register is conditional. Black et al teaches that decrementing of counter register 37 is unconditional. Black et al states at column 10, lines 63 to 65 and at column 11, lines 25 to 28:

> "In the PowerPC Architecture, branch unit 20 decrements the value of counter register 37 at the beginning of the execution stage of each branch instruction."

In accordance with this disclosure of Black et al, the decrement or modification of counter register 37 is not conditioned upon the condition of a conditional branch instruction as required by claims 1 and 10. Thus claims 1 and 10 are not anticipated by Black et al.

Claim 2 recites subject matter not anticipated by Black et al. Claim 2 recites "conditionally decrement the operand." Black et al teaches decrementing counter register 37 for every branch instruction. Thus claim 2 is allowable over Black et al.

New claims 15 to 17 and 20 to 22 recite subject matter not disclosed in Black et al. Claims 15 and 20 recite that the instruction designates a general purpose register as the test register. This is disclosed in the application at page 22, line 27 to page 23, line 5 in conjunction with Figure 5. Note the dst field (bits 23 to 27) of the conditional branch-decrement instruction illustrated in Figure 5 as the dst field of other instructions illustrated in Figures 3A to 3I. The text at page 17, lines 2 to 11 make clear that this dst field refers to one of the registers of the corresponding register file. New claims 16 and 21 recite that a general purpose register is selected as the predicate register. Claims 17 and 22 recite that the predicate register is selected from a subset of the general purpose registers. This subject matter is disclosed in the application at page 17, line 19 to 28 and Table 5 on page 18. Black et al teaches that counter

register 37 and condition register 39 differ from general purpose registers 32. Note that paragraph 24 of the OFFICE ACTION recognizes that branch unit 20 including counter register 37 and condition register 39 is a different structure than general purpose registers 32. Accordingly, claims 15, 16, 17, 20, 21 and 22 are allowable over Black et al.

Claims 18, 19, 23 and 24 recite subject matter not disclosed in Black et al. Claims 18 and 23 recite fetch packets of a predetermined plurality of instructions on predetermined address boundaries and that the branch address is the sum of the displacement and the predetermined address boundary of the last fetch packet. Claims 19 and 24 recite execute packets that can span fetch patch and that a conditional branch-decrement instruction in a latter fetch packet computes the branch address from the address boundary of the second fetch packet if the second fetch packet contains the conditional branch-decrement instruction. The fetch packets are disclosed in the application at page 18, lines 4 to 6. Computation of the displacement relative to the fetch packet boundary even if the conditional branch-decrement instruction is in a second fetch packet is in the application at page 23, lines 6 to 19. Black et al fails to disclose fetching plural instructions in a fetch packet, nor the predetermined address boundaries.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527